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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,697	10/07/2003	Choong Un Lee	054358-5017	3567

9629 7590 09/21/2006

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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,697	LEE ET AL.	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-12,16 and 17* is/are allowed.

6)☒ Claim(s) *1,3-7 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) None

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Amendment filed June 28, 2006.

Accordingly, claims 1, 3-13, 16 and 17 were amended, and claims 2, 14 and 15 were cancelled. Currently, claims 1, 3-13, 16 and 17 are pending in this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodera et al. (Kodera, USPN 6,195,149 B1) in view of Hadoka et al. (Hadoka, JP 09-325328) and Shiraishi (USPN 6,864,947 B2).

Re claim 1, as shown in Figs. 28-31 (Fig. 30 is annotated), Kodera discloses a method of fabricating a liquid crystal display (LCD) panel, comprising:

forming a plurality of upper LCD panel sections (in sealing-in areas 117) on a first mother substrate 101 and a plurality of LCD panel sections (in sealing-in areas 117) on a second mother substrate 104 (col. 1, lines 22-26);

forming sealant patterns 106 on at least one of the mother substrates 101 and 104 (col. 1, lines 26-28);

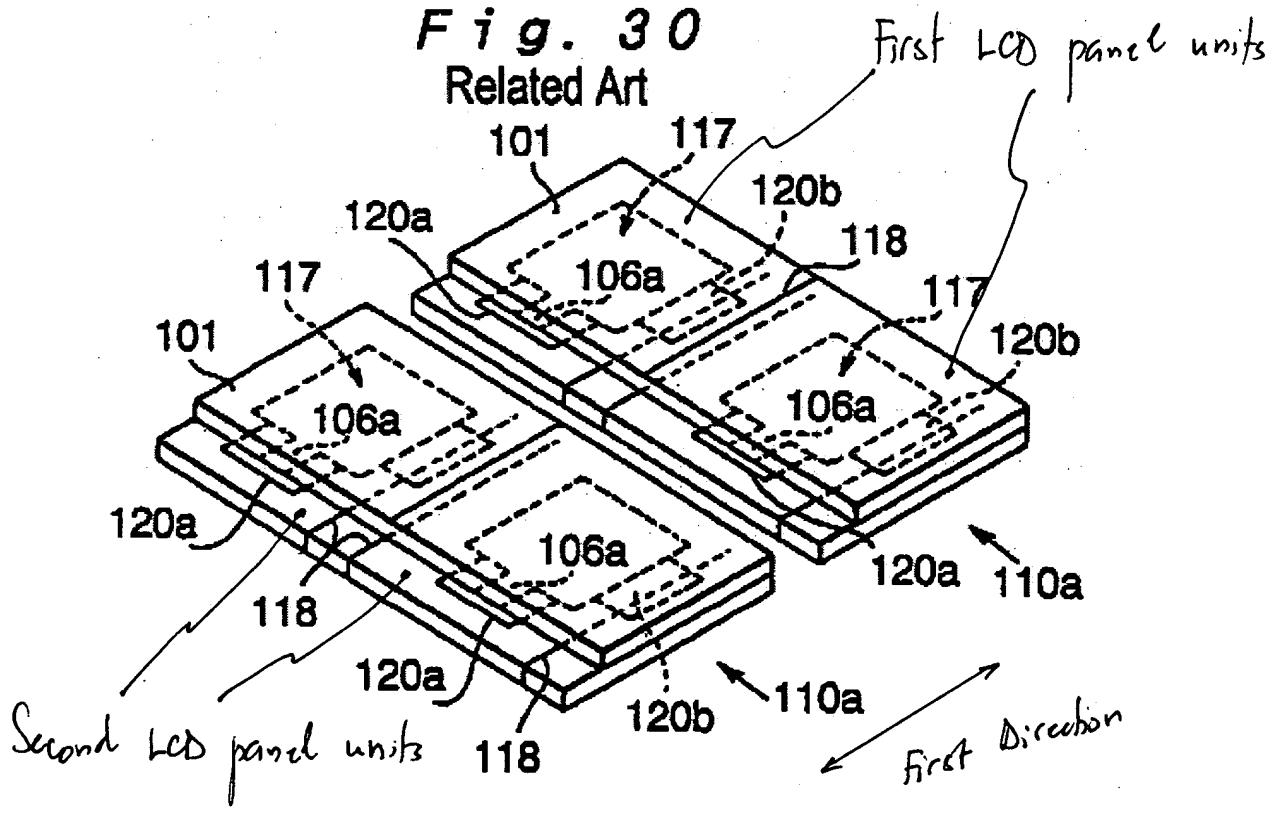
attaching the first and second mother substrates 101 and 104 to each other to bond the upper LCD panel sections with associated ones of the lower LCD panel

sections to form at least first and second LCD panel units 117 (Fig. 30 and col. 1, lines 28-32);

forming at least (first) cutting lines 108 and 118 on each of the first and second mother substrates 101 and 104 the (first) cutting lines 108 and 118 corresponding to a boundary of the first and second LCD units 117 (col. 1, lines 36-60); and

separating the first and second liquid crystal display panel units into individual LCD panels 119 (Fig. 31 and col. 1, lines 60-63).

It is noted that, as shown in Figs. 28 and 30, the cutting lines 108 and 118 create a plurality of dummy sections between the LCD panel units 117.



However, Kodera does not disclose that the LCD panel units having at least two different sizes, wherein first LCD panel unit is larger than the second LCD panel unit; and

second cutting lines are formed on each of the first and second mother substrates, the second cutting lines corresponding to a boundary of the second LCD panel unit,

wherein the first cutting lines extend over at least one sealant pattern; and

wherein the first and second mother substrates include a plurality of dummy sections, each dummy section including main dummy portion and second dummy portion, and at least one of the sealant patterns under the first cutting lines binds the main dummy portions and secondary dummy portions together during the separating step.

At first, as shown in Fig. 1 (annotated), Hakoda discloses a method of fabricating liquid crystal display panels comprising forming first liquid display panel units 3 and second liquid crystal display panel units 4 on a mother substrate 1, wherein the first liquid crystal display panel unit 3 is larger than the second crystal display panel unit 4 (Abstract and Detail Description, paragraphs 7-9).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of fabricating liquid crystal display panels of Kodera with the teaching of Hakoda by forming liquid crystal display panel units having at least two different sizes on mother substrates in order to reduce production cost (Abstract). It is also obvious that second cutting lines are definitely

required to separate the second liquid crystal display panel units into four individual TFT panels 4; accordingly, the second cutting lines are spanning only a portion of the first and second mother substrates and corresponding to a boundary of the second liquid crystal display units.

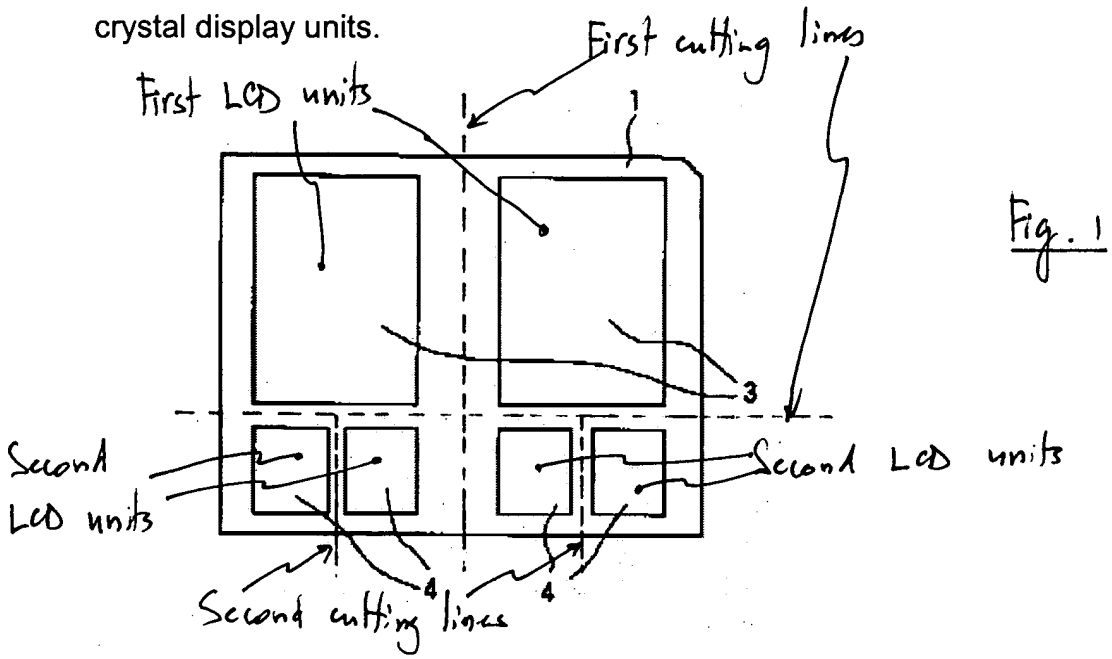


Fig. 1

Further, as shown in Figs. 7A, 7B, 8A and 8B (Fig. 8B is annotated), Shiraishi discloses a method of fabricating a liquid crystal display panel, comprising:

forming cutting lines (scribe cracks) A-L on each adhesive surface of the first mother substrate and second mother substrates 11 and 12 (col. 8, lines 45-51), the cutting lines A-L corresponding to a boundary of the liquid crystal display panel unit 20a (Figs. 7A and 7B); note that the cutting lines A-D, G-J are formed substantially in the first direction (vertical direction in Fig. 8A) and spanned the entire width of the first and second mother substrates 11 and 12; and

separating the liquid display panel units into individual liquid crystal display panels 20a,

wherein the cutting lines A-F extend over sealant pattern 2 (Figs. 8A and 8B); and

wherein, as shown in the annotated Fig. 8B, the first and second mother substrates 11 and 12 include a plurality of dummy sections, each dummy section including main dummy portion and second dummy portion, and at least one of the sealant patterns 21 (dummy patterns) under the cutting lines A-F binds the main dummy portions and secondary dummy portions together during the separating step. Shiraishi discloses that the sealant pattern 21 is provided in order to prevent the bias of the stress when cutting the substrates (col. 10, lines 50-52).

FIG. 8B

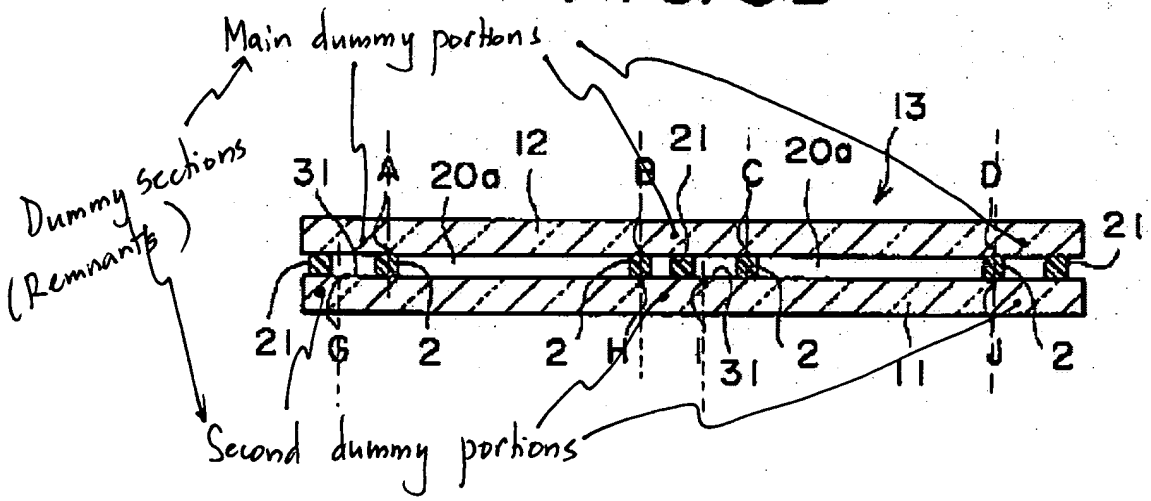


Fig. 8B also shows that the main dummy portions and the secondary dummy portions are formed between the liquid crystal display panel units 20a.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the method of fabricating the liquid crystal display panels of Kodera with the teaching of Shiraishi by extending the cutting lines over the sealant pattern in order to obtain an appropriate cutting surface without receiving an influence of the bias of the stress due to the sealant pattern as well as to enlarge the liquid crystal display areas (col. 5, lines 21-24 and col. 11, lines 3-20).

Re claim 3, Shiraishi discloses that a distance between a terminal face of the sealant 2 and a terminal face of one of the substrates 11 and 12 is substantially equal to or less than 0.5 mm (see also Fig. 3 and col. 6, lines 17-25). Accordingly, this corresponds to the width of the main dummy glass substrates shown in the annotated Fig. 8B. Since the secondary dummy glass substrates is equal to or smaller than the main dummy glass substrates as shown in Fig. 8B, the width of the secondary dummy glass substrates is also substantially equal to or less than 0.5 mm, which meets a width of less than 3 mm of claims 3 and 10.

Re claim 4, Shiraishi discloses that the sealant patterns 21 are formed on non-display regions of the liquid crystal display panels 20a as shown in Fig. 8A.

Re claim 5, Shiraishi discloses that the sealant pattern 21 is positioned on both the main dummy glass substrates and the second dummy glass substrates as shown in Fig. 8B.

Re claims 6 and 11, Fig. 8B of Shiraishi shows that sizes of the upper liquid crystal display panel units on the first mother substrate 12 and the lower liquid crystal

display panel units on the second mother substrate 11 facing correspondingly at into each other are substantially the same.

Re claim 13, as shown in Fig. 10, the method of Shiraishi further comprises injecting liquid crystals into the separated liquid crystal panel units (col. 11, lines 21-28).

Re claim 7, as shown in Fig.11, Kodera discloses every limitations comprising the second substrates 4 having a plurality of thin film transistors and a plurality of pixel electrodes 7, and the first substrates 1 having a common electrode 2 (col. 3, lines 38-52 and col. 8, lines 29-64) except for a plurality of color filters formed on the first substrates. However, it is well known in the art that a plurality of color filters can be formed on the first substrates in order to realize a color display as disclosed by Shiraishi (col. 1, lines 21-26).

Response to Arguments

3. Applicant's arguments filed December 08, 2005 have been fully considered but they are not persuasive.

Applicant argued that Kodera and Shiraishi both fail to teach or suggest at least a "first and second mother substrates include a plurality of dummy sections, each dummy section including a main dummy portion and a secondary dummy portion as recited in claim 1.

The Examiner disagrees with Applicant's remarks since Fig. 8B (annotated) of Shiraishi clearly shows that the first and second mother substrates include a plurality of dummy sections, each dummy section including a main dummy portion and a secondary dummy portion.

Also, Hakoda is employed for teaching a mother glass substrate 1 comprising a plurality of LCD panel sections having at least two different sizes for reducing the production cost as shown in Fig. 1, where the mother glass substrate is cut into LCD units 3 and 4 (see Abstract).

Allowable Subject Matter

4. Claims 8-12, 16 and 17 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claims 8 and 16, none of the prior art of record discloses, in combination with other limitations as claimed, a method of fabricating LCD panels comprising remnants of the separated mother substrates include main dummy portions and secondary dummy portions divided by the first cutting lines therebetween as recited in claim 8, and remnants of the first and second substrates include at least one main dummy portion and at least one secondary dummy portion divided by the first set of cutting lines therebetween as recited in claim 16.

The most relevant reference, US 6,864,947 B2 to Shiraishi, fails to disclose or suggest the remnants including main dummy portions and secondary dummy portions divided by the first cutting lines therebetween. As shown in Fig. 8B, Shiraishi discloses remnants including main dummy portions and secondary dummy portions separated from the mother substrates 11 and 12 respectively by the cutting lines A-D, G-J.

However, these cutting lines are not between the main dummy portions and the secondary dummy portions.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached at (571) 272-1787.

Thoi Duong

09/12/2006

DUNG T. NGUYEN
PRIMARY EXAMINER